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CHARME 2005

CONFERENCE ANNOUNCEMENT

13TH ADVANCED RESEARCH
WORKING CONFERENCE
ON CORRECT HARDWARE DESIGN
AND VERIFICATION METHODS

3 - 6 October 2005

Victor's Residenz-Hotel
66117 Saarbrücken (Germany)

<http://www.charme2005.com>

Co-sponsored by the SIG-CHARME
of IFIP TC10/WG10.5
Special Interest Group on
Formal Design and Verification Methods for
Correct Hardware-like Systems



PRELIMINARY PROGRAMME

Monday, Oct 3

- 08:30 Tutorials, Tools, and Demos
- 10:00 Coffee Break
- 10:30 Tutorials, Tools, and Demos
- 12:00 Lunch Break
- 13:30 Tutorials, Tools, and Demos
- 16:00 Coffee Break
- 16:30 Tutorials, Tools, and Demos
- 17:30 End

Tuesday, Oct 4

- 08:30 Invited Talk

FUNCTIONAL APPROACHES TO DESIGN DESCRIPTION

- 09:30 Wired: Wire-aware Circuit Design
Emil Axelsson, Koen Claessen, and Mary Sheeran
- 10:00 Formalization of the DE2 Language
Warren A. Hunt, Jr., and Erik Reeber
- 10:30 Coffee Break

GAME SOLVING APPROACHES

- 11:00 Finding and Fixing Faults
Stefan Staber, Barbara Jobstmann, and Roderick Bloem
- 11:30 Verifying Quantitative Properties Using Bound Functions
Arindam Chakrabarti, Krishnendu Chatterjee, Thomas A. Henzinger, Orna Kupferman, and Rupak Majumdar
- 12:00 Lunch Break

ABSTRACTION

- 13:30 How Thorough is Thorough Enough?
Arie Gurfinkel and Marsha Chechik
- 14:00 Interleaved Invariant Checking with Dynamic Abstraction
Liang Zhang, Mukul R Prasad, and Michael Hsiao
- 14:30 Automatic Formal Verification of Liveness for Pipelined Processors with Multicycle Functional Units
Miroslav N. Velev
- 15:00 Coffee Break

ALGORITHMS AND TECHNIQUES FOR SPEEDING (DD-BASED) VERIFICATION I

- 15:30 Efficient Symbolic Simulation via Dynamic Scheduling, Don't Caring, and Case Splitting
Viresh Paruthi, Christian Jacobi, and Kai Weber
- 16:00 Achieving Speedups in Distributed Symbolic Reachability Analysis through Asynchronous Computation
Orna Grumberg, Tamir Heyman, Nili Ifergan, and Assaf Schuster
- 16:30 Saturation-based Symbolic Reachability Analysis Using Conjunctive and Disjunctive Partitioning
Gianfranco Ciardo and Jinqing Yu
- 17:00 **Poster Session I**
- 19:00 End

Wednesday, Oct 5

REAL TIME AND LTL MODEL CHECKING

- 08:30 Real-Time Model Checking is Really Simple
Leslie Lamport
- 09:00 Temporal Modalities for Concisely Capturing Timing Diagrams
Hana Chockler and Kathi Fisler
- 09:30 Regular Vacuity
Doron Bustan, Alon Flaisher, Orna Grumberg, Orna Kupferman, and Moshe Y. Vardi
- 10:00 Coffee Break

ALGORITHMS AND TECHNIQUES FOR SPEEDING VERIFICATION II

- 10:30 Automatic Generation of Hints For Symbolic Traversal
David Ward and Fabio Somenzi
- 11:00 Maximal Input Reduction of Sequential Netlists via Synergistic Reparameterization and Localization Strategies
Jason Baumgartner and Hari Mony
- 11:30 A new SAT-based Algorithm for Symbolic Trajectory Evaluation
Jan-Willem Roorda and Koen Claessen
- 12:00 Lunch Break
- 13:30 **Conference Trip**
UNESCO World Cultural Heritage
Völklinger Hütte
- 19:00 Conference Dinner

Thursday, Oct 6

EVALUATION OF SAT-BASED TOOLS

- 08:30 An Analysis of SAT-based Model Checking Techniques in an Industrial Environment
Nina Amla, Xiaoqun Du, Andreas Kuehlmann, Robert P. Kurshan and Kenneth, L. McMillan
- 09:00 **Round Table Discussion**
- 10:30 Coffee Break
- 11:00 **Poster Session II**
- 12:00 Lunch Break

MODEL REDUCTION

- 13:30 Exploiting Constraints in Transformation-Based Verification
Hari Mony, Jason Baumgartner, and Adnan Aziz
- 14:00 Identification and Counter Abstraction for Full Virtual Symmetry
Ou Wei, Arie Gurfinkel, and Marsha Chechik
- 14:30 Coffee Break

VERIFICATION OF MEMORY HIERARCHY MECHANISMS

- 15:00 On the Verification of Memory Management Mechanisms
Iakov Dalinger, Mark Hillebrand, and Wolfgang Paul
- 15:30 Counterexample Guided Invariant Discovery for Parameterized Cache Coherence Verification
Sudhindra Pandav, Konrad Slind, and Ganesh Gopalakrishnan
- 16:00 Closing session